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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,994	10/17/2001	Makoto Nagata	50006-128	4496

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EXAMINER
WEST, JEFFREY R

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/977,994	Applicant(s) NAGATA ET AL.
	Examiner Jeffrey R. West	Art Unit 2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4 and 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The fourth reference listed in the Information Disclosure Statement filed, April 23, 2002, "LEMINGS: LSI's EMI-Noise Analysis With Gate Level Simulator" has not been considered because it has already been cited in the Information Disclosure Statement filed November 29, 2001.

Specification

3. The disclosure is objected to because of the following informalities:

On page 1, line 16, "in a operation speed" should be —in an operation speed—.

The language on page 3, lines 18-20, is confusing.

Appropriate correction is required.

Claim Objections

4. Claims 2 and 9 are objected to because they recite the language "in each segment" before a segment is defined. It is suggested that Applicant reword claims 2 and 9 so that the recitation, "where the digital circuit is divided into a plurality of segments . . ." appears before the language "in each segment".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 1-6 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment" in view of Shimazaki et al., "LEMINGS: LSI's EMI-Noise Analysis with Gate Level Simulator".

Nagata discloses a method for performing measurements and analyses of substrate noise waveform in mixed signal integrated circuit environment comprising representing the integrated circuit according to a distribution of switching operations of a plurality of logic gates and a time series of statically-charged parasitic capacitors connected between a source line and a ground line (page 577, column 1, paragraph 5 and Figure 7). Nagata then discloses generating an analysis module by coupling one end of the group of capacitors with a parasitic impedance of the source line, and connecting the other end of the group of capacitors with a parasitic impedance of the ground line (Figure 7). Nagata also discloses that the source current from the analysis model along with the parasitic impedances of the source and ground lines causes a voltage variation, regarded as substrate noise (page 576, column 1,

paragraph 3, page 577, column 1, paragraph 4, and Figure 5). Nagata further discloses that a value for the parasitic capacitances is determined every predetermined time interval wherein the time interval is set according to the switching operations of the logic gates (page 577, column 2, paragraph 2 to page 578, column 2, paragraph 2). Also, although not specifically disclosed, it is considered inherent that the time interval is shorter as the frequency of the switching operations is greater since frequency and time have an inverse relationship.

With respect to claims 2 and 9, Nagata discloses assigning the group of parasitic capacitors to a group of logic gates wherein the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally appended (i.e. increased) (Figures 7a-c and page 577, column 2, paragraph 2).

With respect to claims 5 and 12, Nagata discloses that the capacitance of the parasitic capacitor to be charged is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed (page 577, column 2, paragraph 2 and equation (2)) (input capacitances, $C_{In,i}$ and $C_{Ip,j}$, and output capacitances $C_{jn,i}$ and $C_{jp,j}$).

Nagata, however, presents the voltage variation as a measure of noise and doesn't specifically disclose determining the waveform of the source current in the digital circuit from the analysis model.

Shimazaki teaches a method for noise analysis comprising determining the noise of an integrated circuit by creating a gate-level simulation of the integrated circuit (2.1) and from it determining an estimate current waveform for noise analysis (2.3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata to include determining the waveform of the source current in the digital circuit from the analysis model, as taught by Shimazaki, because, as suggested by Shimazaki, the combination would have provided a means for conveniently determining the EMI noise characteristics from the current waveform in a time-reducing method (2.6 and 2.7).

Further, Applicant admits as well known in the art, in the Background of the Invention, that "the principal cause of substrate noise generation is a change in voltage generated when the source current of the digital circuits flowing through internal power-supply and ground wirings, which connect the external power supply to the LSI chip, interacts with the parasitic impedances parasitic on those wirings" (page 2, lines 15-20) and "As clearly understood, the generation of noises largely depends on a change in the source current" (page 3, lines 1-2). *When applicant states that something is prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejections. In re Nomiya, 509 F.2d 566, 184 USPQ 607, 610 (CCPA 1975).*

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et

al. in view of Shimazaki et al. and further in view of Mitra et al., "Substrate-Aware Mixed Signal Macrocell Placement in WRIGHT".

As noted above, the invention of Nagata and Shimazaki teaches many of the features of the claimed invention including performing noise analysis on previously designed circuit as well as suggesting that the current analysis method can aid designers in integrated circuit quality (Shimazaki et al., abstract) but does not specifically disclose the method for designing the semiconductor integrated circuit comprising receiving the design information, designing analog and digital circuit according to the design specifications, and re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of substrate noise analysis.

Mitra teaches a computer-implemented method for handing substrate-coupled switching noise in a typical IC containing both sensitive analog and noisy digital circuits (abstract) comprising first receiving minimal area and wire length design specifications, designing the circuits based on the design specifications, and from the design determining the current substrate noise. Mitra then teaches re-designing, based on the substrate noise results, the circuits and guard ring/band positions to obtain acceptable substrate noise results (page 275, column 2, paragraph 3 to page 276, column 1, paragraph 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata and Shimazaki to include a method for designing the semiconductor integrated circuit comprising receiving the design information,

designing analog and digital circuit according to the design specifications, and re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of substrate noise analysis, as taught by Mitra, because, as suggested by Mitra, the combination would have provided a method for incorporating a simplified switching noise estimation into a simulated annealing placement algorithm to allow substrate design that can be used during the design wherein efficient evaluation is critical, but much information about the final chip remains unavailable (page 277, column 1).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure:

Su et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits" teaches an experimental technique for observing the effects of substrate noise as well as approaches to reducing substrate crosstalk.

U.S. Patent No. 5,300,798 to Yamazaki et al. teaches a semiconductor integrated circuit device wherein, to increase analog signal processing accuracy, the impedance of parasitic capacitance between parallel wirings is lowered to account for an increase in signal frequency.

9. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
November 26, 2002